09/808114

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Docket No.: M4065.0381/P381
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Leonard Forbes et al.

Patent No.: 6,734,510 B2

Issued: May 11, 2004

For: TECHNIQUE TO MITIGATE SHORT CHANNEL EFFECTS WITH VERTICAL GATE TRANSISTOR WITH DIFFERENT GATE MATERIALS

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322 & 1.323

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted a typographical error which should be corrected.

In the Specification applicants made the following typographical error:

Column 3, line 17, "conducing" should read --conducting--.

In the Claims, please replace Claim 1 and Claim 32 with the following amended claims:

1. (Amended) A semiconductor device comprising:

a substrate having at least two spaced doped source/drain regions, said source/drain regions defining a channel region therebetween; and

a transistor gate over said substrate and wholly between said spaced doped source/drain regions, said transistor gate having one first gate electrode of a first conductivity type and two second gate electrodes of a second conductivity type, wherein said two second gate electrodes are provided on either side of said first gate electrode [,] and are separated from said first gate electrode by an insulating dielectric layer.

32. (Amended) A semiconductor device, comprising:

a semiconductor substrate, said substrate having at least two separated doped source/drain regions;

three gate electrodes over said substrate and at least partially between said source/drain regions, including a center gate electrode of P+ type conductivity and two adjacent outer gate electrodes of N+ type conductivity;

a gate dielectric separating said three gate electrodes from said substrate;

a thin dielectric layer separating said outer gate electrodes from said center gate electrode;

a first conductive cap layer over said [three vertical] center gate electrode[s, said] and a second conductive cap layer electrically connecting said [three vertical] outer gate electrodes; and

insulating sidewalls adjacent to said conductive cap layer and said outer gate electrodes.

The claims were amended by applicants on April 4, 2003 in response to the Office Action dated December 4, 2002 (Paper No. 9). Accordingly, these claim errors are

PTO errors. Please charge our Credit Card in the amount of $100.00 covering the fee set forth in 37 CFR 1.20(a). Credit Card Payment Form SB-2038, with a signature from an authorized cardholder, is enclosed.

The errors now sought to be corrected are inadvertent typographical errors the correction of which does not involve new matter or require reexamination. The claims, as corrected, were allowed in the Office Action dated June 19, 2003. Claim 32 was listed at that time as Claim 33.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 04-1073, under Order No. M4065.0381/P381.

Dated: September 20, 2005

Respectfully submitted,

By_____

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PTO/SB/44 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,734,510 B2

APPLICATION NO. : 09/808,114

ISSUE DATE : May 11, 2004

INVENTOR(S) : Leonard Forbes et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification:

Column 3, line 17, "conducing" should read --conducting--.

In the Claims, replace Claim 1 and Claim 32 with the following amended claims:

1. A semiconductor device comprising:

a substrate having at least two spaced doped source/drain regions, said source/drain regions defining a channel region therebetween; and

a transistor gate over said substrate and wholly between said spaced doped source/drain regions, said transistor gate having one first gate electrode of a first conductivity type and two second gate electrodes of a second conductivity type, wherein said two second gate electrodes are provided on either side of said first gate electrode and are separated from said first gate electrode by an insulating dielectric layer.

32. A semiconductor device, comprising:

a semiconductor substrate, said substrate having at least two separated doped source/drain regions;

three gate electrodes over said substrate and at least partially between said source/drain regions, including a center gate electrode of P+ type conductivity and two adjacent outer gate electrodes of N+ type conductivity;

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SEP 27 2005

a gate dielectric separating said three gate electrodes from said substrate;

a thin dielectric layer separating said outer gate electrodes from said center gate electrode;

a first conductive cap layer over said center gate electrode and a second conductive cap layer electrically connecting said outer gate electrodes; and

insulating sidewalls adjacent to said conductive cap layer and said outer gate electrodes.

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PTO/SB/17 (12-04v2)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($) 100.00

Complete if Known	
Application Number	Patent#: 6,734,510 B2
Filing Date	Issued: May 11, 2004
First Named Inventor	Leonard Forbes
Examiner Name	K. V. Quinto
Art Unit	2826
Attorney Docket No.	M4065.0381/P381

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 04-1073 Deposit Account Name: Dickstein Shapiro Morin & Oshinsky LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below
☐ Charge fee(s) indicated below, **except for the filing fee**
☐ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17
☒ Credit any overpayments

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims	Fee ($)		Fee Paid ($)
_____	- =	_____	x _____	=	_____

Indep. Claims		Extra Claims	Fee ($)		Fee Paid ($)
_____	- =	_____	x _____	=	_____

Multiple Dependent Claims Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof	Fee ($)		Fee Paid ($)
_____	- 100 =	_____	/50	_____ (round up to a whole number) x	_____	=	_____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): ~~1811~~ Certificate of correction	100.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 28,371	Telephone (202) 828-2232
Name (Print/Type)	Thomas J. D'Amico		Date September 16, 2005